IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

MEDIATEK, INC.,	§	**Civil Action NO. 6:05 CV 323 (LED)**
Plaintiff	§	**Judge: Hon. Leonard Davis**
vs.	§	**Markman Hearing Date: November 21, 2006**
SANYO ELECTRIC CO. LTD. and SANYO NORTH AMERICA CORPORATION,	§	**Trial Date: May 14, 2007**
Defendants.	§	

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In addition to the arguments presented in its opening brief, MediaTek, Inc. ("MediaTek") respectfully submits this reply brief in support of its proposed claim interpretations for U.S. Patent Nos. 5,845,819 ("the '819 Patent"), 6,118,486 ("the '486 Patent"), and 5,751,356 ("the '356 Patent") (collectively "the patents-in-suit").

MediaTek respectfully submits that its constructions are appropriate both in light of the claim language and the specification. Sanyo's own cited law confirms that MediaTek's approach is the correct one: In *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005), the court rejected a formulaic approach to claim construction, stating instead that "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Id.* at 1316. Therefore, although patent claims must be interpreted in light of the specification, which MediaTek has done in its opening brief, it is inappropriate to ignore the claim language in order to obtain a narrower construction. Here, as demonstrated in MediaTek's opening brief, the intrinsic evidence confirms that the ordinary meaning of the claim limitations should control their construction. In contrast, Sanyo's constructions should be rejected because they are overly limited and legally improper.

Sanyo complains that it has not had access to the inventors of the patents-in-suit. Inventor testimony, however, is considered extrinsic evidence. *See Phillips*, 415 F.3d at 1317. Although extrinsic evidence may be helpful in understanding the relevant art, it is less significant than the claim language, patent specification, and prosecution history, which comprise the intrinsic evidence, in determining the meaning of the claim language. *Id.*

I. THE '819 PATENT

Sanyo's constructions for the '819 patent import more structure from the specification that is necessary to perform the claimed functions. Means-plus-function claim limitations, which are construed pursuant to 35 U.S.C. § 112, ¶ 6, are construed differently than ordinary claim limitations. Specifically, the function of the limitation is determined, and then all of the structure

disclosed in the specification that performs that function is identified. *Asyst Techs. Inc. v. Empak, Inc.*, 268 F.3d 1364, 1374–76 (Fed. Cir. 2001). Aspects of the structure unrelated to the claimed function are not "corresponding" and therefore are not a proper part of the construction. *Micro Chemical, Inc. v. Great Plains Chemical Co., Inc.*, 194 F.3d 1250, 1258 (Fed. Cir. 2002). Sanyo's claim constructions, however, improperly import portions of the structure unnecessary to perform the claimed function.

A. Frequency domain down mixing means (Claims 1 and 6)

The claimed function of the frequency domain down mixing means, which is "processing [the] frequency domain audio data so as to mix the audio signals of [the] plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio," speaks for itself. Sanyo, however, proposes changes that modify the meaning of this term. For example, without any support Sanyo replaces "so as to" with "by" "in an attempt to remove complication." These two terms, however, have very different meanings. Stating that the frequency domain down mixing means processes "frequency domain audio data so as to mix the audio signals," as the claim states and MediaTek proposes, indicates that the processing of the frequency domain audio data is done for the purpose of mixing the audio signals. Stating that the frequency domain down mixing means processes "frequency domain audio data by mixing the audio signals," as Sanyo proposes, indicates that the mixing is done for the purpose of processing the frequency domain audio data. Sanyo cites no support for so deviating from the claim language.

In its identification of the structure corresponding to this limitation, Sanyo attempts to expand the structure to include the specific input and output paths and the specific data that can be found on those paths. The structure corresponding to a means-plus-function limitation, however, is only that structure necessary to perform the claimed function. *See Micro Chemical, Inc. v. Great Plains Chemical Co., Inc.*, 194 F.3d 1250, 1258 (Fed. Cir. 2002). By attempting to

limit the structure to the context in which it is disclosed in Figures 7 and 8, Sanyo includes limitations not necessary to perform the claimed function of "processing [the] frequency domain audio data so as to mix the audio signals of [the] plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio." For example, Figure 7 shows the frequency domain down mixing means 40 as being connected to an inverse quantizing circuit 32. The claimed function of the frequency domain down mixing means, however, does not mention inverse quantizing or require that the data be received from the inverse quantizing means. Therefore, consistent with the law, MediaTek's construction includes only that structure necessary to perform the claimed function.

Sanyo further seeks to require that frequency domain down mixing circuit implement equation 4, citing *WMS Gaming v. Int'l Game Tech.*, 184 F.3d 1339 (Fed. Cir. 1999). *WMS Gaming* addresses a case in which the function of a means-plus-function term was implemented in software using a computer or microprocessor. *Id.* at 1349. The '819 Patent, however, leaves open the possibility that the frequency domain down mixing means would be implemented in hardware. Therefore, to the extent that the functionality of the frequency domain down mixing means is implemented in hardware, requiring that hardware to implement the algorithm disclosed in the patent is unsupported by the law.

Sanyo's attempt to expand the function of the "frequency domain down mixing means" in claim 6 is a thinly veiled attempt to invalidate that claim. The function of a means plus function limitation generally follows the word "for." *See Lockheed Martin Corp. v. Space Systems/Loral, Inc.*, 249 F.3d 1314, 1320 (Fed. Cir. 2001). Claim 6, however, states that the "frequency domain down mixing means eliminates the audio signal of said at least one channel from targets to be mixed." Sanyo's proposal that this limitation be added to the function of the frequency domain down mixing means unnecessarily limits this limitation's function. Here, the additional "function" identified by Sanyo is merely an operation that the frequency domain down

mixing means performs in one embodiment.

Sanyo uses this expanded function to attempt to invalidate claim 6 by stating that the '819 patent does not disclose corresponding structure to perform its alleged expanded function. If the Court finds that the frequency domain down mixing means claimed in claim 6 should be read to expand the function of the frequency domain down mixing means, the patent discloses sufficient structure to perform this function. Sanyo's selected specification portion demonstrates that the frequency domain down mixing circuit or frequency domain down mixing means "eliminates the audio signal of said at least one channel from targets to be mixed" when it states:

> In order to construct a further inexpensive audio decoder, the frequency base to time base converting circuit 105, fifth memory circuit 115, and time base to frequency base converting circuit 104 in FIG. 8 may be omitted and when the conversion block lengths among the channels do not coincide, it is sufficient to execute a process of eliminating one or more channel having a different conversion block length from the targets of the down mixing process.

(Opening Br., Ex. A, Col. 10:36–43.) In Figure 8, if one were to eliminate the frequency base to time base converting circuit, the fifth memory circuit, and the time base to frequency base converting circuit, the frequency domain down mixing circuit is the remaining structure that would perform this function. Claim 6 confirms this understanding because it uses the frequency domain down mixing means referenced in claim 1 to eliminate the channel. Therefore, the patent leaves no doubt that the frequency domain down mixing circuit or frequency domain down mixing means "eliminates the audio signal of said at least one channel from targets to be mixed" in claim 6. MediaTek therefore respectfully requests that the Court interpret "frequency domain down mixing means" in both claims 1 and 6 to cover the following structures: a frequency domain down mixing circuit; a frequency domain down mixing circuit implementing equation 4; and equivalents.

B. Frequency base to time base converting means (Claims 1, 3, 11, 13, and 16)

Similar to Sanyo's argument with respect to claim 6 for the "frequency domain down

mixing means" limitation, Sanyo's proposed function for "frequency base to time base converting means" in claim 3 inappropriately expands the required function.[1] The function of a means plus function limitation generally follows the word "for." *See Lockheed Martin Corp. v. Space Systems/Loral, Inc.*, 249 F.3d 1314, 1320 (Fed. Cir. 2001). Claim 3, however, states that "said frequency base to time base converting means converts the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to the time domain on the basis of the block length information separated by said separating means." Sanyo's proposal that this limitation be added to the function of the frequency base to time base converting means unnecessarily limits this limitation's function. Here, the additional "function" identified by Sanyo is merely an operation that the frequency base to time base converting means performs in one embodiment.

In claim 11, the claimed function is "converting [the] frequency domain audio data from the frequency domain to a time domain by using a cosine function with respect to each of the audio signals of [the] plurality of channels." Sanyo attempts to read the function to include the limitation that "the frequency base to time base converting means forms a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function." (Opening Br., Ex. D at 4.) Sanyo apparently obtains this limitation from a portion of the claim limitation that states "thereby forming a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function." (Opening Br., Ex. A, Claim 1.) The claimed function of a means plus function term generally extends from the word "for" and excludes any limitation following the word "whereby" because the term "whereby" merely indicates the results of the limitations of the claim. *Lockheed Martin Corp. v. Space Systems/Loral, Inc.*, 249 F.3d 1314, 1320 (Fed. Cir.

[1] Sanyo erroneously contends that MediaTek did not propose a function for the "frequency base to time base converting means" for claim 3. MediaTek's opening brief, however, stated that the appropriate function for claim 3, like claim 1 is "converting the frequency domain audio data processed by [the] frequency domain down mixing means from the frequency domain to a time domain." (Opening Br. at 11–14.)

2001). Although claim 11 uses "thereby," that word likewise is used to introduce the results of the preceding claim limitation. Accordingly, Sanyo's attempt to limit claim 11's function fails.

In proposing a function for claims 13 and 16, Sanyo proposes "ordinary meanings" of certain terms, but does not provide any legal or factual justification for doing so. Therefore, MediaTek respectfully requests that the Court adopt its proposed function for claims 13 and 16, which is taken directly from the claim language and is "converting the frequency domain audio data from the frequency domain to a time domain with respect to each of the audio signals of the plurality of channels."

In proposing corresponding structure for the frequency base to time base converting means, Sanyo seeks to require that the frequency base to time base converting circuits implement equations 2, 5, and 6, again citing *WMS Gaming v. Int'l Game Tech.*, 184 F.3d 1339 (Fed. Cir. 1999). The '819 Patent, however, does not distinguish between implementing the frequency base to time base converting means in hardware or software. Therefore, to the extent that the functionality of the frequency base to time base converting means is implemented in hardware, requiring that hardware to implement the algorithm disclosed in the patent is unsupported by the law.

To the extent that the functionality of the frequency base to time base converting means is implemented in software, however, it can operate according to equations 2, 5, or 6 regardless of the claim in which it appears. Equations 2, 5, and 6, as Sanyo admits, are substantially identical. (Resp. Br. at 21.) Equation 6 is derived from equation 5 and achieves the same goal.[2] (Resp. Br. at 21.) Sanyo, however, argues that the frequency base to time base converting means would operate using equation 2 in claims 1, 3, 13, and 16 or using equation 5 and 6 in claim 11. Sanyo's apparent justification for this distinction is that claim 11 requires the use of a

[2] Sanyo appears to require that the frequency base to time base converting means as used in claim 11 implement both equation 5 and equation 6. These two equations, however, achieve the same objective of performing frequency base to time base conversion. Therefore, implementing them both in the same circuit would be redundant.

symmetrical cosine function. The patent, however, makes clear that the cosine function itself is symmetrical (Opening Br., Ex. C, Col. 15:62–63.), making the distinction between equations 2 and 5 meaningless. Therefore, "frequency base to time base converting means" should be construed to cover the following structures: a frequency base to time base converting circuit; an IMDCT circuit; a frequency base to time base converting circuit implementing equation 2, 5, or 6; an IMDCT circuit implementing equation 2, 5, or 6; and equivalents.

C. Separating means (Claim 3)

The parties agree that the claimed function of the separating means is "separating [the] frequency domain audio data and [the] block length information from [the] encoded data." Sanyo apparently ignores MediaTek's identification of a demultiplexer as corresponding structure for this function. Instead, Sanyo argues that the demultiplexing circuit may work in combination with an inverse quantizing circuit. Sanyo cites Figure 9 as support for its assertion even though Figure 9 only discloses a demultiplexer (DMUX). In addition, however, the specification further discloses that the above corresponding structures may work in coordination with a buffer memory to separate data. (Opening Br., Ex. A, Col. 12:42–48 ("As mentioned above, according to the embodiment, as buffer memories to be used for the separating process . . ., it is sufficient to use three sets of the first to third buffers #1 to #3 in the work buffer 3 . . . .").)

Similar to its arguments in connection with the frequency domain down mixing means, Sanyo further attempts to limit the corresponding structure to the specific context of Figures 7 and 9 despite the fact that the claimed function does not require that context. *See Micro Chemical, Inc. v. Great Plains Chemical Co., Inc.*, 194 F.3d 1250, 1258 (Fed. Cir. 2002) (noting that the structure necessary to perform the claimed function, and nothing more, should be identified). All the claimed function requires is that the separating means separate the frequency domain audio data and the block length information from the encoded data. Requiring that the

separating means be connected in a certain way to the other elements of the device, which is what Sanyo's identification amounts to, would improperly expand the identified structure to include elements irrelevant to the claimed function. MediaTek's construction identifies the exact structure disclosed to perform the claimed function and nothing more, and therefore should be adopted.

D. Down mixing means (Claims 13 and 16)

The claimed function of this term in claim 13 is "processing the time domain audio data," "adding the time domain audio data stored in [the] buffer memory to the time domain audio data output from [the] window applying means thereby mixing the audio signals of [the] plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio," and "outputting the added time domain audio data to [the] buffer memory." The claimed function of this term in claim 16 is "adding the time domain audio data stored in [the] buffer memory to the time domain audio data output from [the] window applying means thereby mixing the audio signals of [the] plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to [the] buffer memory." MediaTek proposes that the Court adopt these claimed functions as corresponding to the down mixing means. Sanyo admits that its proposed functions do not differ substantially from these claimed functions and provides no justification for deviating from the claim language. Therefore, MediaTek's proposed function should be adopted.

Sanyo attempts to limit the corresponding structure to circuits implementing equation (3), stating that this equation is necessary to ensure that the down mixing circuit employs a predetermined level ratio. Regardless of whether equation (3) is part of the corresponding structure, the down mixing means must perform the claimed function, which implements a predetermined level ratio. The issue is whether it must implement that ratio using equation (3) or whether it can use some other equation. Given the language in the specification indicating that

equation (3) is an "example" of such a process, MediaTek respectfully submits that the down mixing circuit is not so limited. (Opening Br., Ex. A at 4:20.)

Sanyo further cites *WMS Gaming v. Int'l Game Tech.*, 184 F.3d 1339 (Fed. Cir. 1999) in support of limiting the down mixing circuit to circuits implementing equation (3). *WMS Gaming* addresses a case in which the function of a means-plus-function term was implemented using software executed on a computer or processor. *Id.* at 1349. The '819 Patent, however, leaves open the possibility that the down mixing means would be implemented in hardware. To the extent that the functionality of the down mixing means is implemented in hardware, requiring that hardware to implement the algorithm disclosed in the patent is unsupported by the law. Therefore, MediaTek respectfully requests that the Court construe the "down mixing means" to cover the following structures: a down mixing circuit; a down mixing circuit implementing equation (3); and equivalents.

II. THE '486 PATENT

The '486 Patent indeed presents an invention that makes a video processing system simpler and cheaper, but, as Sanyo argues, it presents at least four ways to achieve that goal. (Resp. Br. at 10.) The patent claims, not the specification, define the scope of the invention. The appropriate construction of the '486 Patent need not incorporate each and every method for achieving the goal of simplifying the video system. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) presented a similar situation. In that case, the patent-in-suit disclosed several purposes for baffles, including the ability to deflect projectiles. The court's adopted construction, however, included baffles that would not be able to deflect projectiles. *Id.* at 1327. Similarly, the '486 patent presents a number of advantages for the claimed invention. The '486 claims, as demonstrated below, dictate how the patent achieves the goal of simplifying the system. Sanyo, however, seeks to read the specification into the claims to achieve an overly narrow scope.

A. Fixed frequency (Claims 1 and 2)

The term "fixed frequency" (which is found in the patent in the context of the limitation "fixed frequency horizontal deflection signal") should be interpreted to mean "a single frequency," not "a frequency that cannot be changed," as Sanyo proposes. The patent specification states that: "[T]he inventor recognized that further cost savings may be achieved by selecting, for use by a display device, a *single horizontal scanning frequency* . . . ." (Opening Br., Ex. B, Col. 2:42–45 (emphasis added).) Therefore, the patent indicates that the term "fixed frequency" means "a single frequency."

Sanyo's construction of the term is overly restrictive because it requires that the frequency can never be changed. The claims and specification, however, contemplate that the "fixed frequency horizontal deflection signal" be separately derived for each new input video stream, which indicates that the frequency can be changed as long as one frequency is used at a time. In the claims, the term is used in the context of "a fixed frequency horizontal deflection signal," which is generated in response to a raster clock signal, indicating that the display device does not use the same fixed frequency horizontal deflection signal regardless of the input signal. (Opening Br., Ex. B, Claim 1.) The specification confirms this relationship. (Opening Br., Ex. B, Col. 6:40–43 ("Raster generator 190 generates a fixed frequency horizontal deflection signal H-DEF and a vertical deflection signal V-DEF in a conventional manner in response to a raster clock signal f_{RAST}.").) Sanyo, however, argues that this express claim language and reference from the specification should be ignored in light of the prosecution history. In contrast, MediaTek's construction reconciles the three sources of intrinsic evidence, making its construction the most appropriate one. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.").

Sanyo argues that the use of the word "fixed" limits the horizontal deflection signal to

one that cannot be changed. (Resp. Br. at 26–27.) Sanyo further argues that the vertical deflection signal does not use the word "fixed", meaning its frequency can be changed based on the output video signal. In essence, Sanyo draws the distinction between the frequencies of the horizontal and vertical deflection signals by stating the horizontal deflection frequency never changes ("fixed"), while the vertical deflection frequency changes based on the output signal (not "fixed").

But this distinction ignores the language of claim 1. Claim 1 states that the raster clock signal generates both the horizontal and vertical deflection signals. The frequency of those signals will change when the raster clock signal changes (e.g., input video stream change). The reason for the use of the term “fixed” with only the horizontal deflection frequency is because that frequency, unlike the vertical deflection frequency, is not affected by the output video signal. In other words, the vertical deflection frequency is not fixed because it is “defined by a vertical display format of said output video signal.” Thus, claim 1 clearly contemplates that the “fixed frequency horizontal deflection signal” can be separately derived for each new input video stream.

Sanyo’s citation of the prosecution history here is overly restrictive. The patent claims a technology for ensuring that the display device utilizes the same clock as the recording device. As anyone who uses more than one clock can attest, different clocks may run faster or slower than each other: What is counted as one minute on one clock may be counted as only 59.5 seconds on another clock. The ‘486 technology, by deriving the fixed frequency horizontal deflection signal and vertical deflection signal using the raster clock signal, which was created using the program clock reference transmitted by the recording device, ensures that the recording device and the display device are using the same standard of time. This calibration preserves the relationship between the different signals: To use a simplistic example, if the system clock signal is supposed to be 27 MHz and the fixed frequency horizontal deflection signal is supposed

to be 270 MHz, deriving the fixed frequency horizontal deflection signal each time a new PCR is received ensures that the two signals maintain their relative values. In contrast, the vertical deflection signal might vary widely for different input signals with different display formats.

Sanyo's treatment of the prosecution history further conflates claim interpretation with infringement under the doctrine of equivalents, which is the relevant context for prosecution history estoppel. Sanyo states that MediaTek is estopped from arguing that the frequency of the horizontal deflection signal changes with the input signal,[3] citing *Sextant Avionique v. Analog Devices, Inc.*, 172 F.3d 817 (Fed. Cir. 1999). *Sextant Avionique*, however, makes clear that prosecution history estoppel relates to determining infringement under the doctrine of equivalents. *Id.* at 825–26. Indeed, the court in *Sextant Avionique* treated the prosecution history, like the patent specification and claims, as evidence of the appropriate scope of a claim limitation for purposes of claim interpretation, not as creating a claim construction estoppel. *Id.* at 825. Therefore, MediaTek respectfully requests that the Court interpret "fixed frequency" to mean "a single frequency."

B. Raster clock signal (Claims 1 and 2)

MediaTek's construction of "raster clock signal" remains true to the ordinary meaning of the term, the specification, and the claim language. The ordinary meaning of the "raster clock signal" as demonstrated by the specification is a "display clock," which, for clarity, MediaTek has defined as "a periodic signal used to synchronize a display device." (Opening Br., Ex. B, Col. 8:6–8 ("To reduce system cost and complexity, the DTV receiver 100 of FIG. 1 utilizes a non-standard frequency for raster clock f_{RAST} (i.e., the display clock) . . . .").) Sanyo provides no evidence to demonstrate that this is not the ordinary meaning.

Instead, Sanyo argues that the patentee acted as his own lexicographer in defining the raster clock signal. Nowhere, however, does the patentee explicitly redefine the term "raster

[3] MediaTek also disputes that prosecution history estoppel would apply to this term for purposes of infringement under the doctrine of equivalents.

clock signal" to have a "non-standard frequency easily derived." Sanyo cites one example from Column 8, which describes the preferred embodiment disclosed in Figure 1 as using a non-standard frequency. (Opening Br., Ex. B, Col. 8:6–8.) In addition, Sanyo's quotation from the invention summary only states that the display raster signals "do not *need* to conform to the waveforms commonly used . . . ." and that "intervention contemplates the use of other native display formats and other raster frequencies." (Opening Br., Ex. B at 2:33–35 (emphasis added).) These quotations, far from narrowing the meaning of the raster clock signal, in fact expand it to include a variety of waveforms. The specification, therefore, does not forbid the raster clock signal from having a non-standard frequency.

Requiring the raster clock signal to have a non-standard frequency would import limitations from the specification into the claims without justification. While recognizing the importance of the specification in interpreting the claims, the *Phillips* Court distinguished between construing terms in light of the specification and importing limitations from the specification into the claims. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005). The Court stated:

> [T]he line between construing terms and importing limitations can be discerned with reasonable certainty and predictability if the court's focus remains on understanding how a person of ordinary skill in the art would understand the claim terms. For instance, although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.

Id. Therefore, the focus in claim construction should be on how one of skill in the art would read the claim limitations, not on limiting the claim language to the embodiments disclosed in the specification. Therefore, consistent with the claim language, MediaTek's respectfully requests that the Court construe "raster clock signal" to mean "a periodic signal used to synchronize a display device."

C. Clock circuit (Claim 1)

Sanyo's proposed construction for clock circuit is based on an overly restrictive reading of the specification. Sanyo attempts to limit the term to a preferred embodiment in the specification with only one voltage controlled oscillator ("VCO"). (Opening Br., Ex. B, Col. 4:36–51.) Notably, the specification states that the example is only illustrative. *Id.*[4] As further evidence, Sanyo cites various sections of the specification that describe the use of a single VCO as being "advantageous." The patented technology, however, has many advantages, and therefore the claims need not be restricted to require the implementation of all of the advantageous characteristics. (Opening Br., Ex. B., Col. 2:33–53.) *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1326–27 ("We have held that 'the fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives.'"). Therefore, it would be inappropriate to require the clock circuit to contain only one VCO.

D. Frequency scaling (Claims 1 and 2)

Sanyo's proposed construction for frequency scaling is based in large part on the baseless assertion that multiplying the frequency of a signal by any factor other than two is "difficult."[5] (Resp. Br. at 39–40.) Sanyo cites no intrinsic or extrinsic evidence to support this statement. To the contrary, Sanyo's construction is improper because its own intrinsic evidence contradicts it. Claim 1 states that "said raster clock signal [is] generated by frequency scaling said system clock signal," indicating that the apparatus uses the system clock signal to generate the raster clock signal. Sanyo's own intrinsic evidence states:

[4] Sanyo's other "evidence" of the scope of this term has been modified for Sanyo's purposes. For example, Sanyo cites column 13, lines 60–64 as supporting its position that the clock circuit may only have one VCO. That portion of the specification, however, only states that "The above-described invention advantageously provides for a DTV receiver having a single master clock producing a raster or pixel clock from which a 27 MHz system clock and, optionally, an additional decoder clock having a different frequency, is easily synthesized." In its brief, Sanyo attempted to equate the "master clock" with the VCO, without any support from the evidence. Indeed, the "master clock" phrase could refer to the clock circuit itself.

[5] Sanyo has modified its construction from the Joint Claim Construction Statement. In that document, Sanyo admitted that frequency scaling included multiplying a frequency. (Opening Br., Ex. D. at 14.)

> [S]everal of the raster clock frequencies f_{RAST} deemed by the inventor to be useful in practicing the invention are 67.5MHz (5x27 MHz/2) [5:2 ratio], 81 MHz (3x27MHz) [3:1 ratio], 94.5 MHz (7x 27 MHz/2) [7:2 ratio] and 108 MHz (7x27 MHz) . . . .

(Opening Br., Ex. B, Col. 9:28–31.) Therefore, the intrinsic evidence explicitly discloses multiplying the system clock signal frequency by three, five, or seven, not just two, to obtain the raster clock signal.

Similarly, the intrinsic evidence does not support Sanyo's requirement that the frequency be multiplied or divided by an "easily derived value." Certain embodiments of the patent refer to the raster clock frequency, not the factor or factors used in frequency scaling, being "easy to produce" or "easily derived". (Opening Br., Ex. B, Col. 9:31–33; Col. 12:49–52.) Therefore, Sanyo's construction has no basis in the intrinsic evidence, and MediaTek respectfully requests that the Court construe "frequency scaling" to mean "multiplying and/or dividing a frequency by a given factor."

III. THE '356 PATENT

Similar to the '819 Patent, Sanyo's constructions for the '356 Patent import limitations from the cited structure that are unrelated to the claimed functions. Aspects of the structure unrelated to the claimed function are not "corresponding" and therefore are not a proper part of the construction. *Micro Chemical, Inc. v. Great Plains Chemical Co., Inc.*, 194 F.3d 1250, 1258 (Fed. Cir. 2002). Sanyo's claim constructions, however, improperly import portions of the structure unnecessary to perform the claimed function.

A. Video encoding means for encoding a video signal into video data (Claims 1 and 7)

MediaTek has considered and adopted Sanyo's proposed function for this means. In light of this function, MediaTek submits that a video signal encoder including an encoder circuit, a header creation circuit, and a multiplexer circuit is the appropriate corresponding structure. Sanyo's definition of that structure, however, is overly limiting. Sanyo seeks to require that

these circuits implement the MPEG1 or MPEG2 standards, citing *WMS Gaming v. Int'l Game Tech.*, 184 F.3d 1339 (Fed. Cir. 1999). *WMS Gaming* addresses a case in which the function of a means-plus-function term was implemented in software, which is run using a processor or computer. *Id.* at 1349. The '356 Patent, however, does not specify whether the video signal encoder must be implemented in hardware or software. Therefore, to the extent that the functionality of the video encoding means is implemented in hardware, requiring that hardware to implement the algorithm disclosed in the patent is unsupported by the law.

To the extent that the functionality of the video encoding means is implemented in software, however, the algorithm associated with the means should not be limited to MPEG1 and MPEG2. Figure 1 of the patent shows "an arrangement of a video/audio signal coding system according to an embodiment based on an MPEG system." (Opening Br., Ex. C, Col. 3:39–41.) MPEG is broader than MPEG1 and MPEG2. Therefore, Sanyo's proposed structure for the video encoding means should be construed to cover the following structures: a video signal encoder including an encoder circuit, a header creation circuit, and a multiplexer circuit; a video signal encoder including an encoder circuit utilizing the MPEG standard, a header creation circuit, and a multiplexer circuit; and equivalents.

Sub-terms

The terms "data number information," "header information," and "predetermined video data unit" were originally proposed for construction when the parties exchanged such terms many months ago. Indeed, MediaTek prepared and served constructions for these terms on Sanyo. Subsequently, the parties agreed not to construe a large number of terms, including these terms, in favor of letting their ordinary meaning control. Sanyo still chooses to advance constructions for those terms. To the extent that the Court wishes to construe them, MediaTek submits the following.

The term "data number information" should be construed to mean "a value indicative of

the bit length of a picture." This term accords with Sanyo's cited intrinsic evidence. Sanyo's proposed construction for this term imports a number of limitations without providing any support for those limitations. For example, Sanyo attempts to require, without any support, that the "data number information" not be part of the encoded video data. (Resp. Br. at 43.) Sanyo further defines the "data number information" to be a "D value," without any evidentiary support. Therefore, to the extent that the Court wishes to construe "data number information," it should be construed to mean "a value indicative of the bit length of a picture."

The term "predetermined video data unit" should be construed to mean "a predetermined set of pictures." By defining the "predetermined video data unit" in terms of a "group of pictures" ("GOP"), Sanyo's definition attempts to read the terminology of the MPEG standard into the term and thereby limit the patent to its preferred embodiment. The focus of claim construction, however, is to determine what one of ordinary skill in the art would understand the claims to mean. While recognizing the importance of the specification in interpreting the claims, the *Phillips* Court distinguished between construing terms in light of the specification and importing limitations from the specification into the claims. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005). Therefore, "predetermined video data unit" should be construed to mean "a predetermined set of pictures."

The term "header information" should be construed in accordance with its ordinary meaning to mean "data that carries information about video data." Sanyo's definition of this term incorporates its definition of "predetermined video data unit," which Sanyo defines as a GOP. Therefore, Sanyo's definition covers only GOP headers. A patent, however, should not be construed to exclude a preferred embodiment. *Invitrogen Corp. v. Biocrest Mfg., L.P.*, 327 F.3d 1364, 1370–71 (Fed. Cir. 2003). The specification and Sanyo cite sequence headers, GOP headers, and picture headers as examples of "header information" (Resp. Br. at 43; Opening Br., Ex. C, Col. 4:20–25.) Sanyo's construction, however, would only cover the GOP headers and

should be rejected.

B. Audio encoding means (Claims 1 and 7)

Sanyo attempts to require that the audio encoding means implement the MPEG standard, again citing *WMS Gaming v. Int'l Game Tech.*, 184 F.3d 1339 (Fed. Cir. 1999). As with the video encoding means, however, the '356 Patent does not specify whether the audio encoding means would be implemented in software or hardware. Therefore, to the extent that the functionality of the audio encoding means is implemented in hardware, requiring that hardware to implement the algorithm disclosed in the patent is unsupported by the law. *See id.* at 1349.

Sanyo further attempts to require, without any evidentiary support, that the audio signal encoder be separate from the video signal encoder. (Opening Br., Ex. D at 17.) The only alleged support that Sanyo cites in support of its construction is a functional block diagram in the specification, which has separate blocks for the audio signal encoder and video signal encoder. Sanyo can cite to no intrinsic evidence, however, explicitly requiring that the audio signal encoder be separate from the video signal encoder. All corresponding structures are embraced by a means-plus-function limitation, and corresponding structure should be identified with the broadest possible scope. *See Micro Chemical, Inc. v. Great Plains Chemical Co., Inc.*, 194 F.3d 1250, 1258–59 (Fed. Cir. 2002). Therefore, Sanyo's requirement that the audio signal encoder and video signal encoder be separate should be rejected, and the audio encoding means should be construed to cover an audio signal encoder, an audio signal encoder implementing the MPEG standard, and equivalents.

C. System header generating means (Claim 1)

The claimed function of the "system header generating means" is "generating system headers on the basis of the header information and the data number information stored in [the] first memory." The function of a means-plus-function term should be the claimed function. *See Micro Chemical, Inc. v. Great Plains Chemical Co., Inc.*, 194 F.3d 1250, 1257–58 (Fed. Cir.

2002). Sanyo, however, further complicates the function to require that the means generate a "complete" system header "without processing the encoded video data stream output from the video signal encoder."

This construction presents two problems. First, Sanyo cites no support from the intrinsic evidence justifying importing the limitation that the system header be "complete," instead relying on the inapposite statement that "The processor 4 writes the created system header in the header information memory 5." (Opening Br., Ex. C, Col. 5:10–11.) Given that this statement does not even mention that the system header would be "complete," it is difficult to imagine how it justifies adding the word "complete" to the function. Second, Sanyo unnecessarily qualifies the claimed function by requiring that the system header be generated "without processing the encoded video data stream output from the video signal encoder." Indeed, MediaTek's claimed function itself states that the system header is generated based on the header information and the data number information stored in the first memory. Therefore, Sanyo appears to be taking a "belt-and-suspenders" approach by requiring that the system header be generated "without extracting the video header information from the bit stream." The claim states the function best: the system header generating means' function is "generating system headers on the basis of the header information and the data number information stored in said first memory." Therefore, consistent with the claim language and specification, MediaTek respectfully requests that the Court adopt its proposed construction for "system header generating means."

D. Multiplexing means (Claim 1 and 7)

Sanyo's identification of corresponding structure for the multiplexing means is overly limited. Sanyo departs from its argument in the Joint Claim Construction Statement that only the entire multiplexer can perform the claimed function (Opening Br., Ex. D at 18.), now arguing that only a "discrete multiplexing circuit" can perform the claimed function. As a preliminary matter, Sanyo inserts the word "discrete" into the structure without providing any justification

for doing so. Further, both a multiplexer and a multiplexer circuit alone are expressly associated with multiplexing in the patent specification, making both structures appropriate corresponding structures for this claim element. (Opening Br., Ex. C, Col. 5:23–25 ("The compressed video and audio data, as well as a data signal such as text information . . . are input to the multiplexer 7 to be integrated and create a single train or stream of data.").) Therefore, consistent with the claim language and specification, MediaTek respectfully requests that the Court adopt its proposed construction for "multiplexing means."

E. System header (Claims 1, 4, and 7)

The term "system header" should be construed in accordance with its ordinary meaning, which is "data that carries information about the audio and video streams." Sanyo does not dispute that the system header carries information about the audio and video streams, but argues, without justification from the specification, that "system header" should be defined to mean "a complete data structure that is combined with the combined encoded video and audio data streams." Sanyo's cited intrinsic evidence does not require that the "system header" be a "complete data structure" and only contains information about where the system header is stored, not how it is combined with the audio and video data streams. (Resp. Br. at 49.) Therefore, MediaTek respectfully requests that the Court construe "system header" to mean "data that carries information about the audio and video streams."

IV. CONCLUSION

Sanyo improperly attempts to limit the patent claims to the preferred embodiments. MediaTek's constructions, however, remain true to both the claim language and the specification. Therefore, for the reasons stated above and in MediaTek's opening brief, MediaTek respectfully requests that the Court adopt its proposed claim constructions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a). As such, this notice was served on all counsel who have consented to electronic service. Local Rule CV-5(a)(3)(A). Pursuant to Fed.R.Civ.P. 5(d) and Local Rule CV-5(e), all other counsel of record not deemed to have consented to electronic service were served with a true and correct copy of the foregoing by U.S. mail, on this 22nd day of September, 2006.

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